Current Trends Towards Energy Efficient Transistors

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An overview will be given on various concepts to improve the energy efficiency of highly scaled transistors. Since 2007 high-k dielectrics, strained Si and Si-Ge have been used to improve the performance. Concomitantly, the dimensions have been downscaled to 28 nm. For the next generations a transition to fully depleted devices has become necessary to minimize deteriorating short channel effects for gate lengths ≤20nm. Two routes are being pursued: Fully depleted SOI transistors with thin box are favored by European semiconductor manufacturers while others prefer FinFETs. One step further, in research, nanowire transistors, inheriting the ultimate MOSFET architecture with high mobility intrinsic channels and best electrostatic gate control, are being investigated. Results of fully depleted SOI transistors as well as nanowire array transistors with typical dimensions of 10-30 nm will be presented. Also for nanowire devices, further improvements of the channel mobility, the high-k/metal gate stacks and the contacts are needed. Examples for strained channel materials and novel gate stacks will be presented.

In addition to these mainstream developments, concepts for more energy efficient devices, so called steep slope devices, will be discussed. In this context, band-to-band tunneling transistors (TFETs) with planar and nanowire architecture will be presented and perspectives for switching at voltages as small as 0.25 V will be discussed. Such devices are most desired for mobile and autonomous systems.

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